SHRI VAISHNAV VIDYAPEETH VISHWAVIDYALAYA
INDORE

Shri Vaishnav Entrance Test (SVET)

Syllabus for PhD (Electronics Engineering)

Section 1:- Logic and Data Interpretation.

Section 2:- Quantitative Skills.

Section 3:- Comprehension and Verbal Skills.

Section 4:- Subject Specific GATE /NET Syllabus in relevant discipline.