B

Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore

Shri Vaishnav Institute of Technology and Science, Indore

Time Table (Regular / ATKT) (Revision 02)
V Semester End Semester Examination Dec. 2024 - Jan. 2025
B.Tech. (All Programs Including Dual Degree)

Time: 09:30 AM to 12:30 PM (Morning Shift)

Date/Day	B.Tech (Electronics & Communications Engineering)	B.Tech (Electronics & Communications Engineering - IOT)	B.Tech (Mechatronics) (Year Back) + ATKT	B.Tech (Electrical Engineering/ Electrical & Electronics)
24-Dec-24	**BTEI401**	**BTEI401**	**BTMT501**	**BTEE501N**
Tuesday	Microprocessor and Microcontroller	Microprocessor and Microcontroller	Applied Hydraulics and Pneumatics	Electrical Machines-II
27-Dec-24	**BTEC502**	**BTECIOT501**	**BTMT611**	**BTEE514**
Friday	Cellular and Mobile Communication	Communication Systems	Robotics and Automation	Introduction of IoT in Electrical Engineering
30-Dec-24	**BTME510**	**BTME510**	**BTME510**	**BTME510**
Monday	Design Thinking and Innovation	Design Thinking and Inovation	Design Thinking and Innovation	Design Thinking and Innovation
1-Jan-25	**BTCS403**	**BTEC515**	**BTCS403**	**BTEE504**
Wednesday	Data Structures and Algorithm	Data Communication and Computer Networks	Data Structures and Algorithm	Switchgear and Protection
3-Jan-25	**BTEC504**	**BTECIOT603**	**BTEE503**	**BTEE503**
Friday	CMOS VLSI Design	IOT Architecture and Protocols	Control System Engineering	Control System Engineering
6-Jan-25				**BTEE502***
Monday				Power Electronics

*Revised

Practical Examination to be held between 06 Dec. to 18 Dec. 2024

***Students are advised to see their internal marks before appearing in the end sem examination**

The syllabus for ATKT students shall be as per the revised (updated) syllabus.

**** Students are advised to see www.svvv.edu.in (University Website) for all informations related Theory exam Time Table (Regular / ATKT)**

Mr. Sunil Pipleya
Asst. COE

Dr. Nilesh Patidar
Asst. COE

Dr. Shishir Jain
Controller of Examinations